AMENDMENTS TO THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Withdrawn; Currently Amended) A method of manufacturing a semiconductor device comprising:

a first step of interposing an adhesive between a surface of a substrate on which an interconnect pattern is formed and a surface of a semiconductor chip on which electrodes are formed, said adhesive having conductive particles dispersed therein; and

a second step in which pressure is applied between said semiconductor chip and said substrate, said interconnect pattern and said electrodes are electrically connected via at least part of said conductive particles of said adhesive, and said adhesive is caused to cover ~~substantially~~ all area of lateral surfaces of said semiconductor chip that is substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed.

2. (Withdrawn) The method of manufacturing a semiconductor device as defined in claim 1,

wherein said adhesive is provided in the first step at a thickness greater than the interval between said semiconductor chip and said substrate after the second step.

3. (Canceled)

4. (Canceled)

5. (Withdrawn) The method of manufacturing a semiconductor device as defined in claim 1,

wherein before the first step, said adhesive is previously disposed on the surface of said semiconductor chip on which said electrodes are formed.

6. (Withdrawn) The method of manufacturing a semiconductor device as defined in claim 1, wherein before the first step, said adhesive is previously disposed on the surface of said substrate on which said interconnect pattern is formed.

7. (Withdrawn) The method of manufacturing a semiconductor device as defined in claim 1, wherein said adhesive includes a shading material.

8. (Currently Amended) A semiconductor device, comprising:

a semiconductor chip having electrodes; a substrate having an interconnect pattern; and an adhesive, said adhesive having conductive particles dispersed therein;

wherein said electrodes and said interconnect pattern are electrically connected via at least part of said conductive particles of said adhesive; and

wherein said adhesive is interposed between a surface of said substrate on which said interconnect pattern is formed and a surface of said semiconductor chip on which said electrodes are formed, and said adhesive covers ~~substantially~~ all area of lateral surfaces of said semiconductor chip that is substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed.

9. (Canceled)

10. (Canceled)

11. (Previously Presented) The semiconductor device as defined in claim 8, wherein said adhesive is provided to cover said interconnect pattern in its entirety.

12. (Previously Presented) The semiconductor device as defined in claim 8, wherein said adhesive includes a shading material.

13. (Canceled)

14. (Currently Amended) A circuit board on which is mounted a semiconductor device, the semiconductor device comprising:

a semiconductor chip having electrodes; a substrate having an interconnect pattern; and an adhesive, said adhesive having conductive particles dispersed therein;

wherein said electrodes and said interconnect pattern are electrically connected via at least part of said conductive particles of said adhesive; and

wherein said adhesive is interposed between a surface of said substrate on which said interconnect pattern is formed and a surface of said semiconductor chip on which said electrodes are formed, and said adhesive covers ~~substantially~~ all area of lateral surfaces of said semiconductor chip that is substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed.

15. (Currently Amended) An electronic instrument having a semiconductor device, the semiconductor device comprising:

a semiconductor chip having electrodes; a substrate having an interconnect pattern; and an adhesive, said adhesive having conductive particles dispersed therein;

wherein said electrodes and said interconnect pattern are electrically connected via at least part of said conductive particles of said adhesive; and

wherein said adhesive is interposed between a surface of said substrate on which said interconnect pattern is formed and a surface of said semiconductor chip on which said electrodes are formed, and said adhesive covers ~~substantially~~ all area of lateral surfaces of said semiconductor chip that is substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed.

16. (Previously Presented) The semiconductor device as defined in claim 8, wherein at least a part of said adhesive has a thickness substantially the same as said semiconductor chip.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Currently Amended) The circuit board as defined in claim 14,

wherein a part of said adhesive covering ~~substantially~~ all area of lateral surfaces of said semiconductor chip has a thickness substantially the same as said semiconductor chip.

22. (Currently Amended) The electronic instrument as defined in claim 15,

wherein a part of said adhesive covering ~~substantially~~ all area of lateral surfaces of said semiconductor chip has a thickness substantially the same as said semiconductor chip.

23. (Withdrawn; Currently Amended) The method of manufacturing a semiconductor device as defined in claim 1,

wherein a part of said adhesive covering ~~substantially~~ all area of said lateral surfaces of said semiconductor chip is formed to have part of said conductive particles dispersed therein.

24. (Currently Amended) The semiconductor device as defined in claim 8,

wherein a part of said adhesive covering ~~substantially~~ all area of said lateral surfaces of said semiconductor chip has part of said conductive particles dispersed therein.

25. (Currently Amended) The circuit board as defined in claim 14,

wherein a part of said adhesive covering ~~substantially~~ all area of said lateral surfaces of said semiconductor chip has part of said conductive particles dispersed therein.

26. (Currently Amended) The electronic instrument as defined in claim 15,

wherein a part of said adhesive covering ~~substantially~~ all area of said lateral surfaces of said semiconductor chip has part of said conductive particles dispersed therein.

REMARKS

Claims 1, 2, 5-8, 11, 12, 14-16 and 21-26 are pending herein. Claims 1, 2, 5-7 and 23 have been withdrawn by way of a Restriction Requirement.

By this Amendment, claims 1, 8, 14 and 15 are each amended to recite that the adhesive covers all area of lateral surfaces of the semiconductor chip, which lateral surfaces are substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed. Corresponding amendments are also made to dependent claims 21-26. These amendments are made in response to the rejections relying upon the newly cited Watanabe reference, as discussed more fully below. No new matter is added by these amendments, support being found in the original specification at least at, for example, Figure 5B and the corresponding description in the specification.

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to the Watanabe reference, which is cited for the first time in the Final Rejection. Entry of the amendments is thus respectfully requested.

In view of the foregoing amendments and the following remarks, reconsideration of this application is respectfully requested.

I. Rejection Under 35 U.S.C. §102(e)

Claims 8, 14-16, 21, 22 and 24-26 were rejected under 35 U.S.C. §102(e) as allegedly being clearly anticipated by U.S. Patent No. 6,077,382 (hereinafter "Watanabe"). This rejection is respectfully traversed.

In each of independent claims 8, 14 and 15, it is required that the adhesive, which is interposed between a surface of the substrate on which an interconnect pattern is formed and a surface of a semiconductor chip in which electrodes are formed, and which has conductive particles dispersed therein, cover all area of lateral (i.e., side) surfaces of the semiconductor chip, which lateral surfaces are substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed. Applicant respectfully submits that Watanabe does not teach or suggest a semiconductor device, circuit board or electronic instrument in which the adhesive joining the semiconductor chip and the interconnect pattern substrate is made to cover all area of lateral surfaces of the semiconductor chip.

In the Office Action, it was alleged that Figs. 1-4, 4-4, 6 and 7-4 of Watanabe anticipate the claims. In these figures, Watanabe illustrates a semiconductor chip 13 having bump electrodes 14 thereon joined to a substrate 12 having wiring patterns 15 formed thereon via an anisotropic conductive adhesive 18. The conductive adhesive includes conductive particles 18a therein. In each of Figs. 1-4, 4-4, 6 and 7-4 of Watanabe, the adhesive 18 is illustrated to cover portions of the lateral surfaces of the semiconductor chip.

In the Office Action, it was asserted that these illustrations in Watanabe showed that the adhesive 18 substantially covered the lateral surfaces of the semiconductor chip 13. However, by this Amendment, each of independent claims 8, 14 and 15 have been amended to require that the adhesive cover all of the lateral surfaces of the semiconductor chip. Nowhere does Watanabe teach or suggest any embodiments in which the adhesive 18 covers all of the lateral surfaces of the semiconductor chip.

As described at the bottom of page 18 of the present specification, by covering all of the lateral surfaces of the semiconductor chip with an anisotropic conductive material, the semiconductor chip can be protected from mechanical damage. Further, corrosion of the electrodes of the semiconductor chip can be prevented. These benefits are nowhere taught or suggested in Watanabe. In fact, Watanabe describes no reason whatsoever for having the adhesive 18 cover portions of the lateral surfaces of the semiconductor chip. In view of this, one of ordinary skill in the art would have had no motivation to have modified the teachings of Watanabe to make the adhesive cover all of the lateral surfaces of the semiconductor chip, rather than just portions of the lateral surfaces. Thus, nothing in Watanabe would have led one of ordinary skill in the art to the presently claimed invention.

For at least the foregoing reasons, Applicant respectfully submits that Watanabe neither teaches nor suggests the presently claimed invention. Reconsideration and withdrawal of this rejection are respectfully requested.

II. Rejections Under 35 U.S.C. §103(a)

A. Watanabe in view of Tsukagoshi

Claim 11 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Watanabe in view of U.S. Patent No. 5,804,882 (hereinafter "Tsukagoshi"). This rejection is respectfully traversed.

The Patent Office correctly noted that Watanabe does not teach or suggest that the adhesive is provided to cover the entirety of the interconnect pattern as required in dependent claim 11. The Patent Office turned to the teachings of Tsukagoshi as allegedly suggesting such embodiment.

However, even if the teachings of Watanabe and Tsukagoshi were to have been combined as alleged in the Office Action, Applicant respectfully submits that the presently

claimed invention still would not have been achieved. Specifically, Tsukagoshi fails to remedy the deficiencies of Watanabe discussed above.

Tsukagoshi describes a semiconductor device in which a semiconductor chip 1 having electrodes 2 to thereon is joined to a substrate 4 having circuits 5 and projecting electrodes 7 thereon by way of an adhesive 11 that includes electroconductive particles 12. However, as clearly shown in Figs. 1-4 and 9 of Tsukagoshi, Tsukagoshi does not teach or suggest that the adhesive must be made to cover all area of lateral surfaces of the semiconductor chip. Thus, Tsukagoshi suffers from the same deficiencies as Watanabe discussed above.

For at least the foregoing reasons, Applicant respectfully submits that the combined teachings of Watanabe and Tsukagoshi fail to teach or suggest the presently claimed invention. Reconsideration and withdrawal of this rejection are respectfully requested.

B. Watanabe in view of Canning

Claim 12 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Watanabe in view of U.S. Patent No. 5,783,465 (hereinafter "Canning"). This rejection is respectfully traversed.

The Patent Office acknowledged that Watanabe failed to teach or suggest that the adhesive should include a shading material as required in dependent claim 12. The Patent Office turned to the teachings of Canning as allegedly remedying this deficiency of Watanabe.

Applicant respectfully submits that even if the teachings of Watanabe and Canning were to have been combined in the manner alleged in the Office Action, the presently claimed invention still would not have been achieved. That is, Canning also fails to teach or suggest providing an adhesive having conductive particles dispersed therein and being configured to cover all area of lateral surfaces of a semiconductor chip.